

PACS

Predictive Acceleration of Critical Section Execution with Asymmetric Multi-Core Architectures

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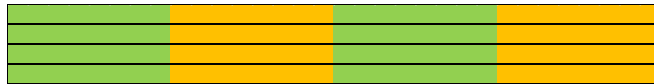
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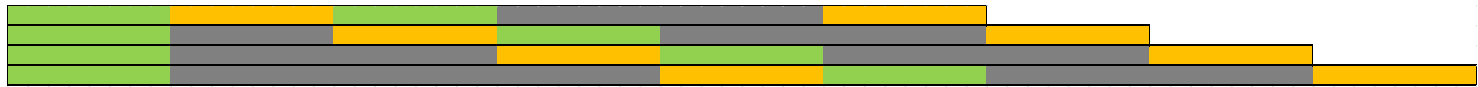
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IDEA

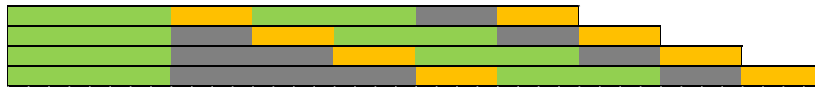
Scenario



Naïve Multicore



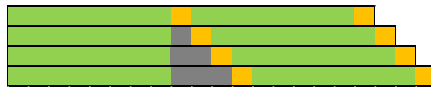
ACS 2x



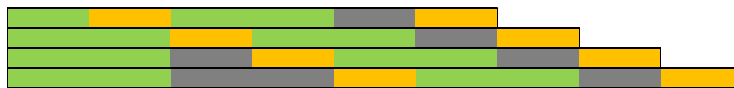
ACS 4x



ACS 8x



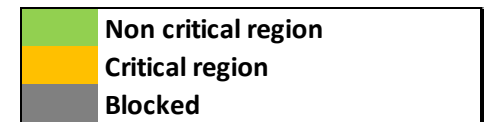
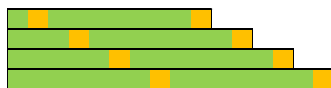
PACS 2x



PACS 4x



PACS 8x



Simulation results for Vanilla trace

- Environment: 4-cores, 1-Fast
- Application: 4-threads, 1-critical region

Speed-up on Fast core	Wait-cycles on ACS	Wait-cycles on PACS
1x	600	600
2x	300	102
4x	150	0

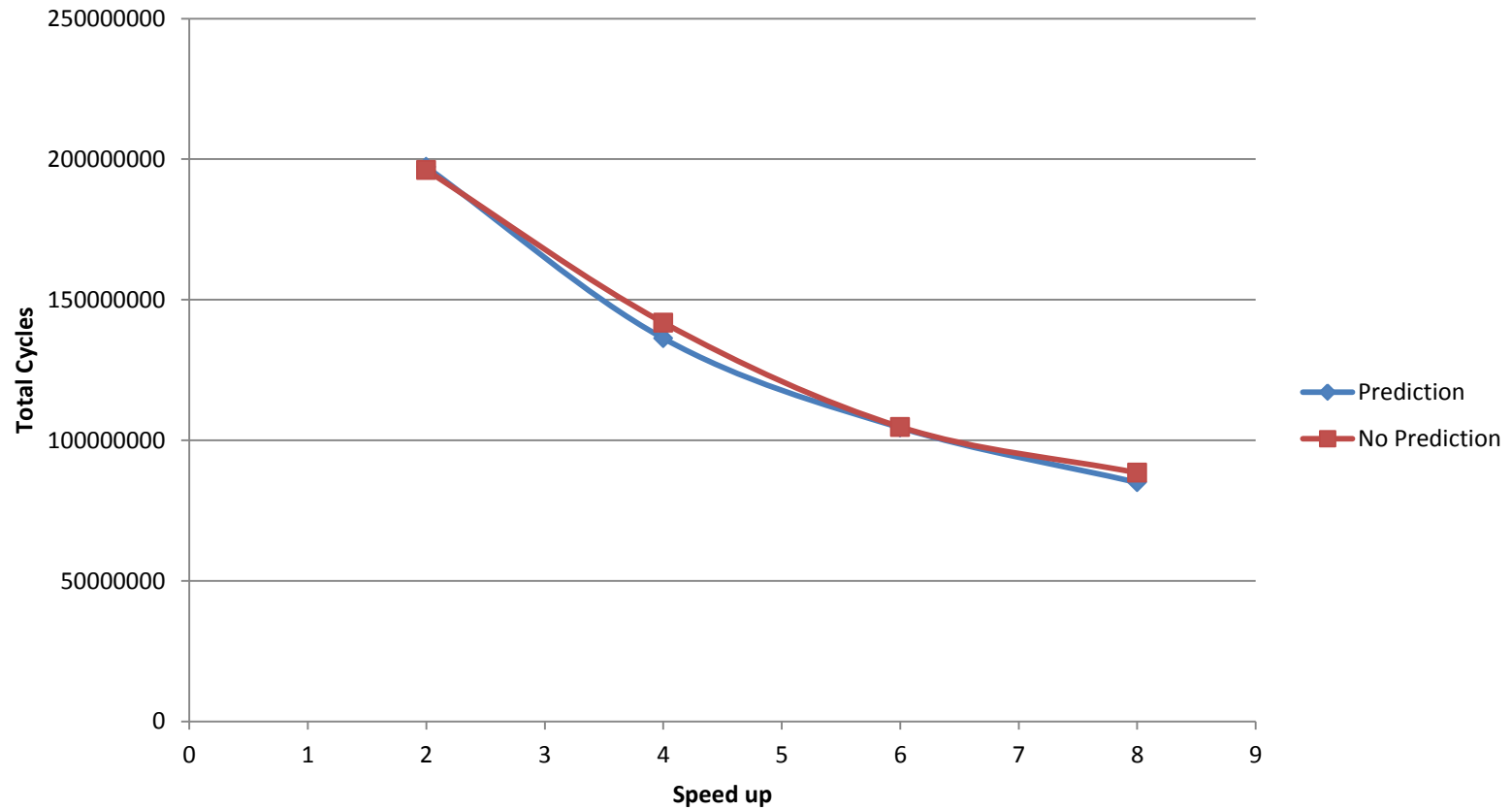
Vanilla Trace:

```
#inst:100
#predict<CR, 100>
#inst:100
Lock<CR>
#inst:100
Unlock<CR>
#inst:100
#release<>
#inst:100
```



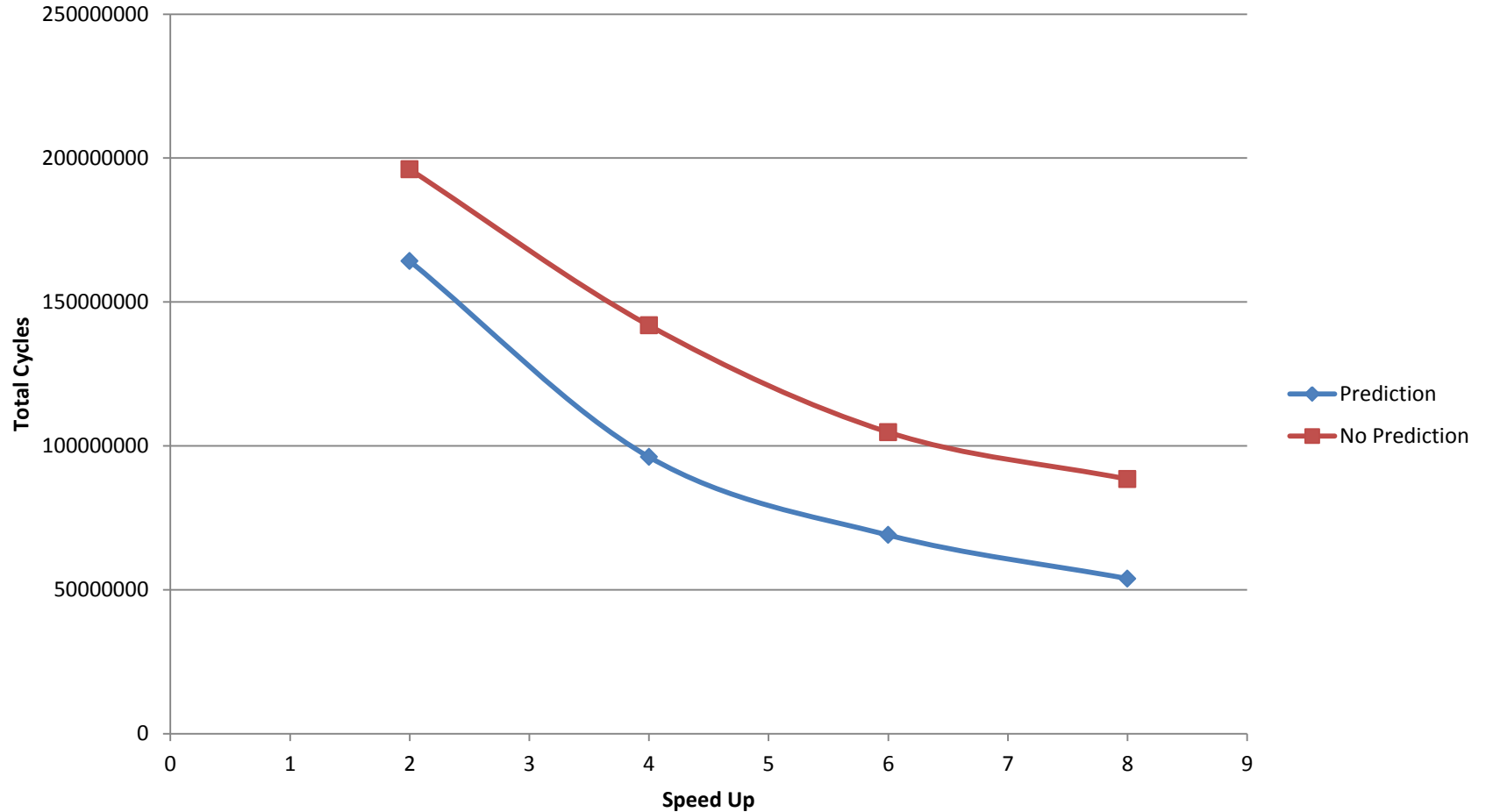
Simulation results on X264 traces

Global Cycles for One Fast Core



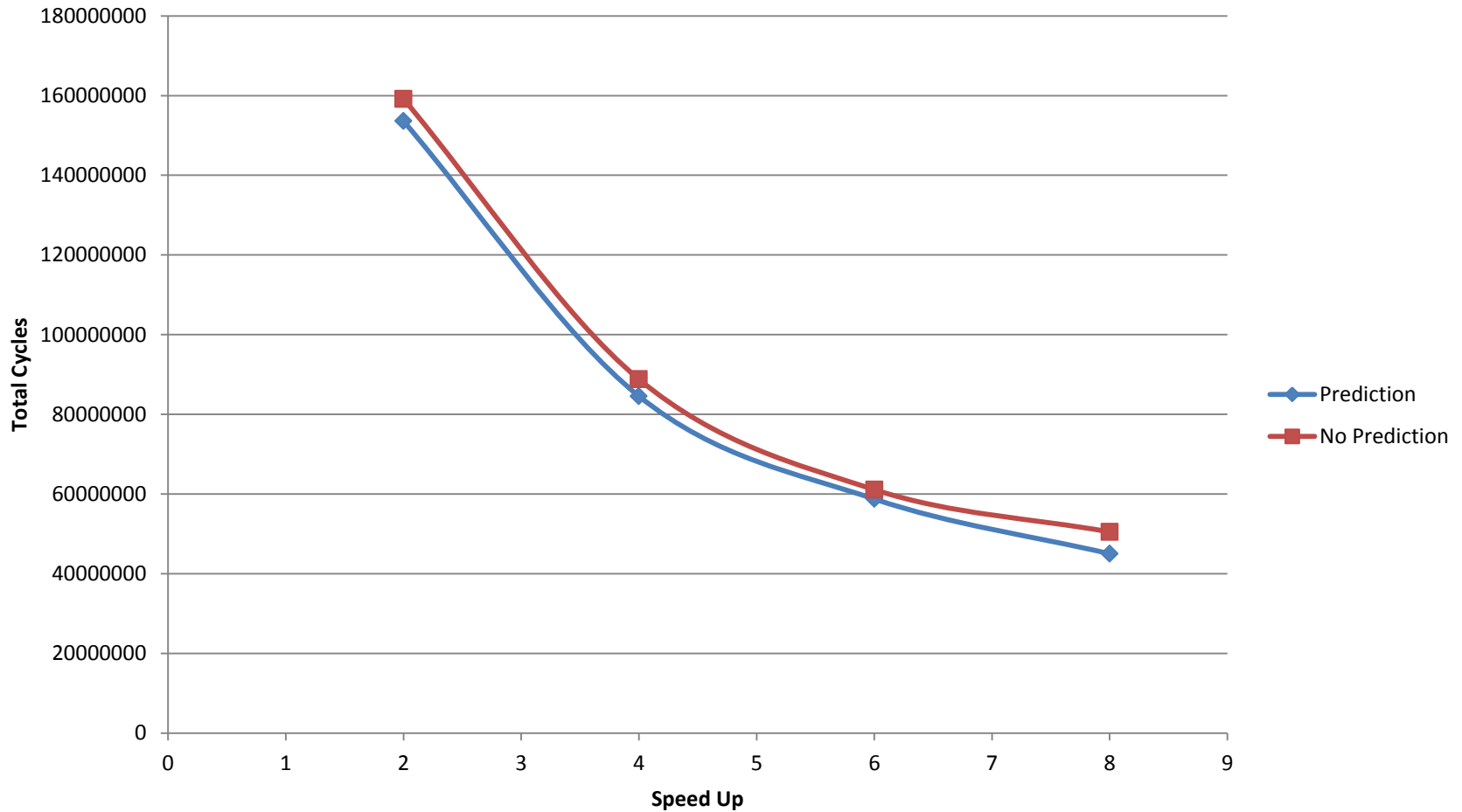
Simulation results on X264 traces

Global Cycles for Two Cores



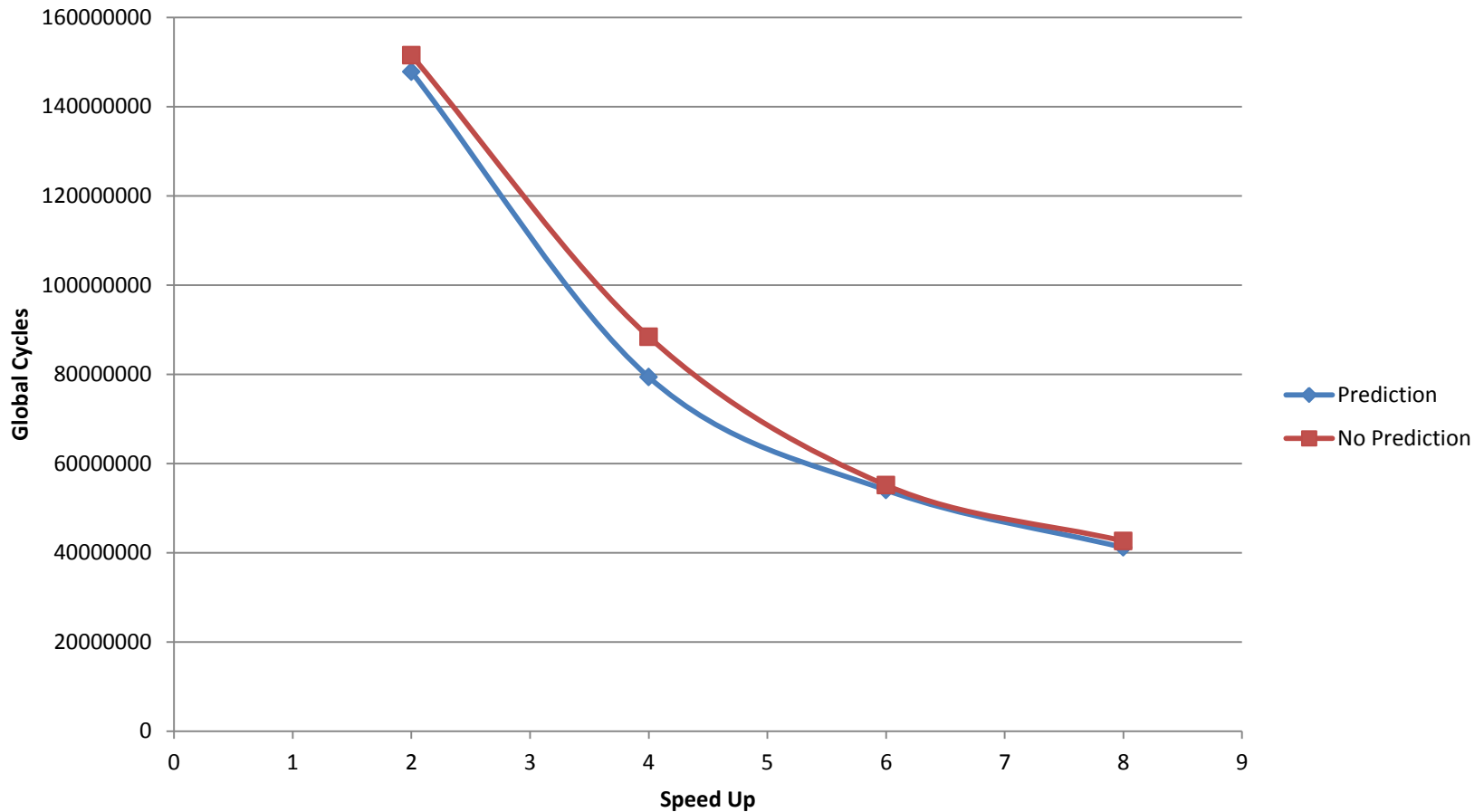
Simulation results on X264 traces

Global Cycles for Three Cores



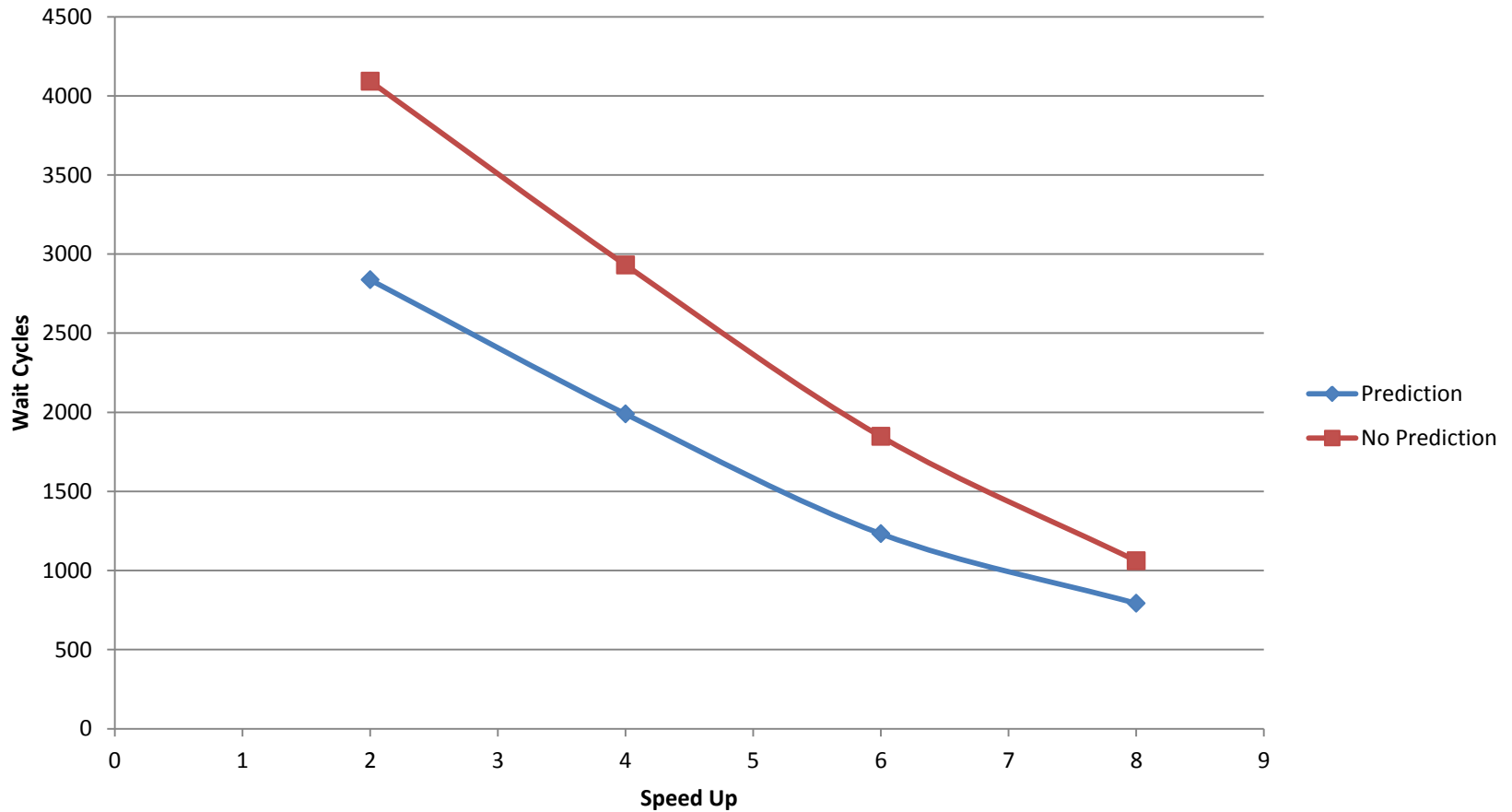
Simulation results on X264 traces

Global Cycles for Four Cores



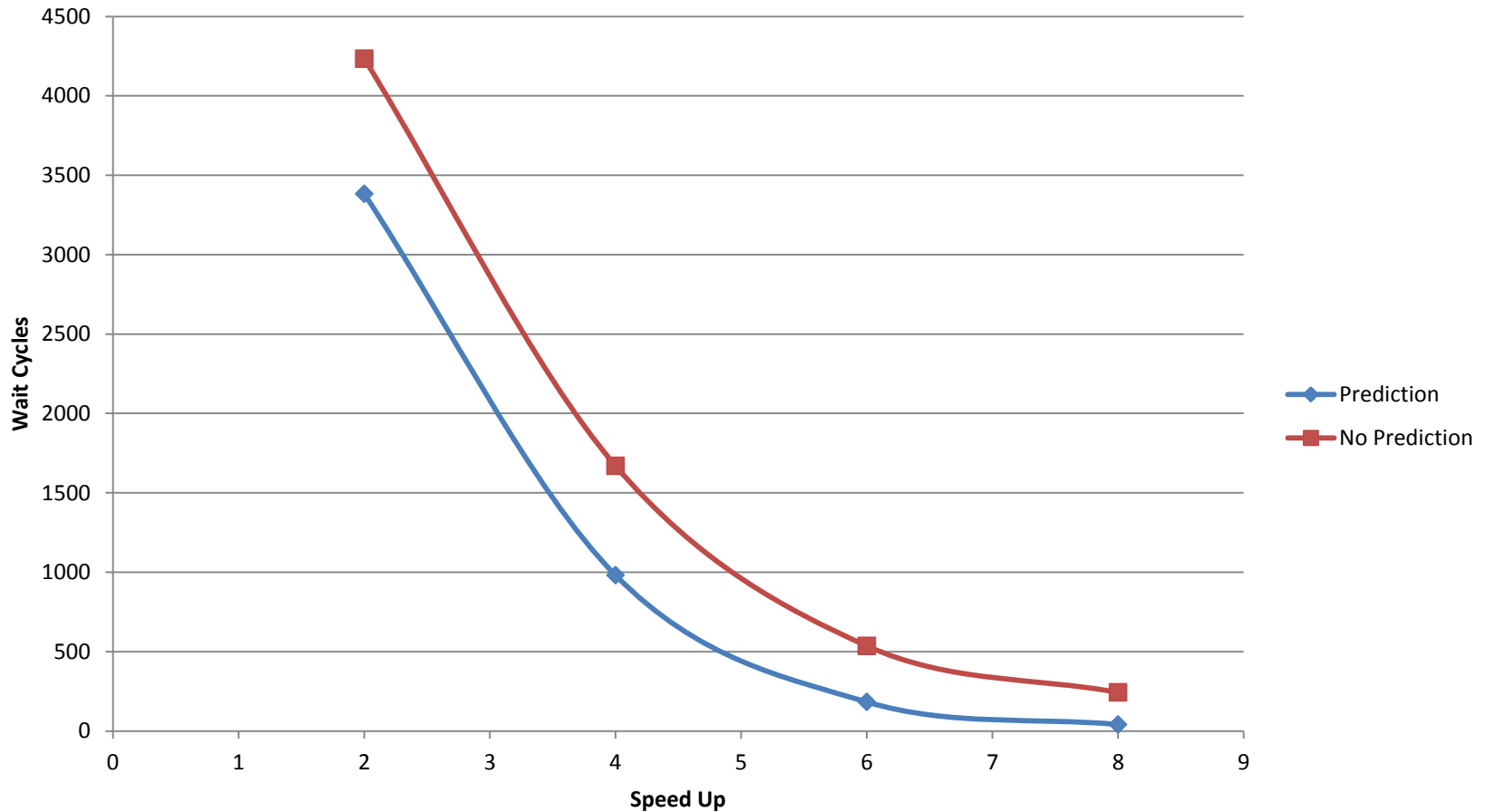
Simulation results on X264 traces

Wait Cycles for One Fast Core



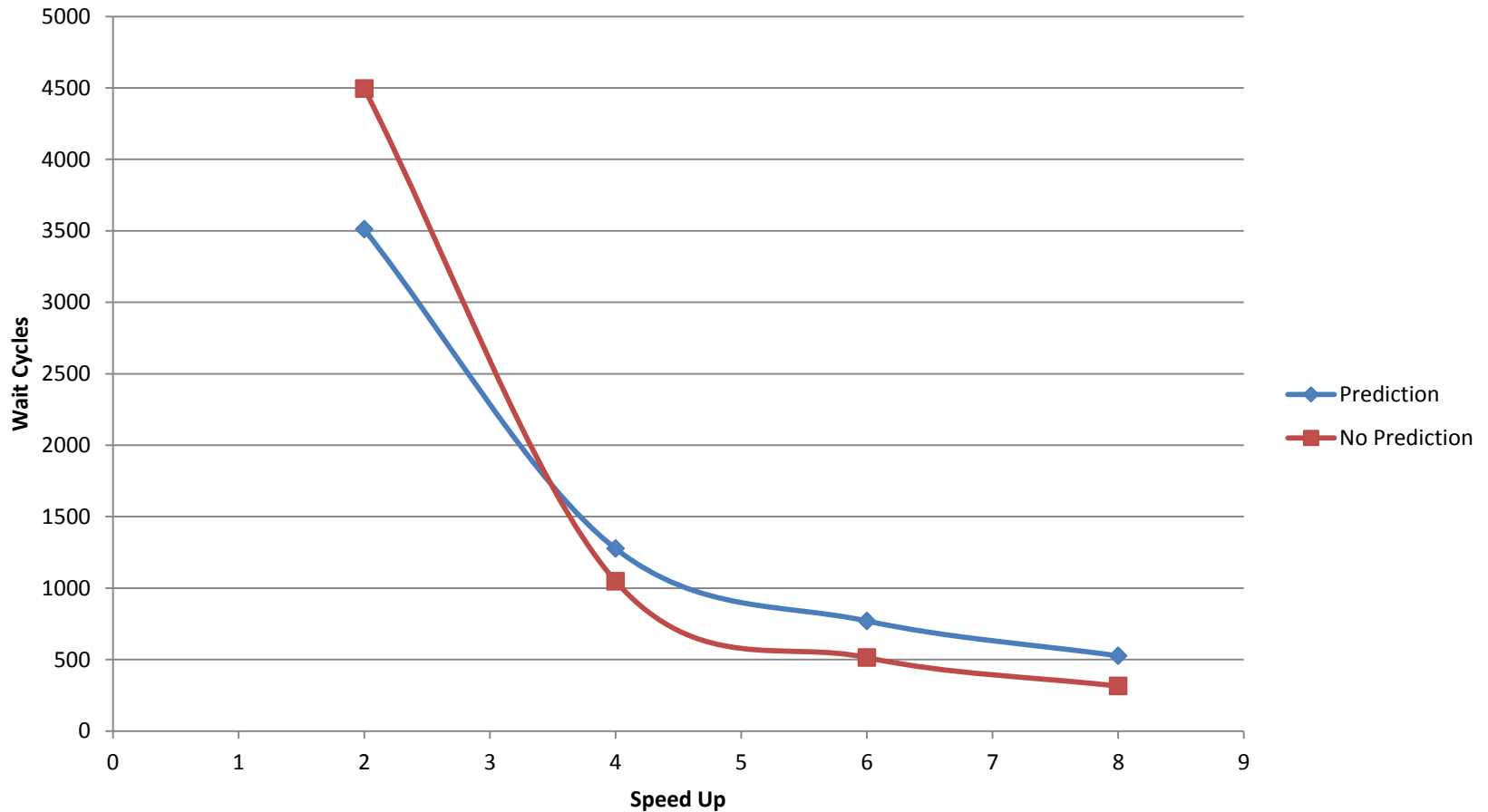
Simulation results on X264 traces

Wait Cycles for Two Fast Cores



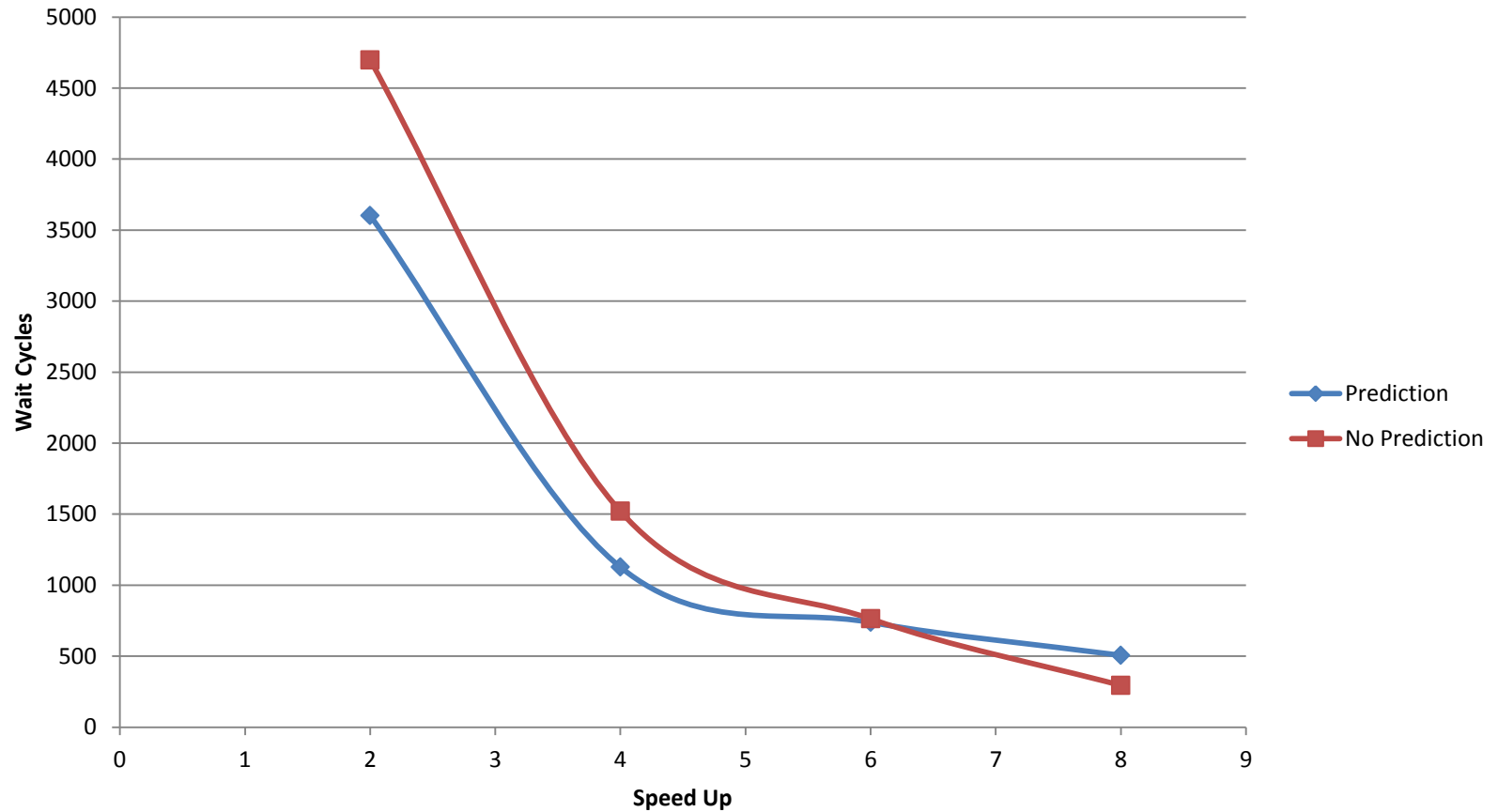
Simulation results on X264 traces

Wait Cycles for Three Fast Cores



Simulation results on X264 traces

Wait Cycles for Four Fast Cores



Reasons for Anomalies

- Contention generated through false prediction

WOLF !!

WOLF !!

- ... or may be a Bug ??

Key Issues to be addressed in Milestone-3

- False predictions
 - Solution?
 - History based credibility prediction
- Late mutex identification
 - Solution?
 - History based mutex prediction